TÉCNICO LISBOA

DIGITAL SYSTEMS

Quarter 2 - 2023/2024 | LEEC, LEAer, LEFT

January 19th, 2024 | Duration: 2h00

Instructions

Before starting the exam, read carefully the following information:

- There are (at least) nine different versions of this exam.
- Although the exam comprises a total of 24 pages, there are two distinct volumes that should be handled as follows:
  - **Volume 1** corresponds to the question list and comprises pages 1 to 20. These pages do not need to be identified because they will be discarded at the end of the exam;
  - **Volume 2** corresponds to the answers sheet and comprises pages 21 to 24. All pages of this volume **MUST** be identified with the **student's name** and **number**.
  - At the end of the exam, all pages of **Volume 2** will be separated. Consequently, all non-identified pages will not be considered.
- The exam is composed of three parts (Part I, II and III) and has a duration of 2 (two) hours.
  - **Part I** comprises N_1 multiple choice questions and awards a total of $P_1 = 15$ points.
    - Each correct answer awards $C = P_1/N_1$ points;
    - Each wrong answer awards $W = -C/(A-1)$ points (negative value), where A denotes the number of possible answers offered to each question;
    - Each non-answered question awards 0 points.
  - **Part II** comprises an open-answer problem about combinatorial circuits and awards a total of $P_2 = 2.5$ points.
  - **Part III** comprises an open-answer problem about sequential circuits and awards a total of $P_3 = 2.5$ points.
  - All question answers **MUST** be replied in the alloted space of **Volume 2**.
- At the end of **Part I of Volume 1** you will find and empty page - you can use it for auxiliary calculations, but this page will not be delivered at the end. This means that all answers **MUST** be replied (and properly justified) in the alloted space of **Volume 2**.
- Each question includes a Portuguese translation of the corresponding text. In case of a mismatch between the English text and its translation, the English text will be the one to be considered in the evaluation[1].
- You cannot use or consult any material during the exam. On your desk you can only have a pen and your student identity card.

[1] Cada pergunta inclui uma tradução para Português do referido texto. Em caso de incoerência entre o texto em Inglês e a sua tradução, será o texto em Inglês que será considerado na avaliação.

Volume 1 - Part I

Question permutation table:

Question	Version	1	2	3	4	5	6	7	8	9
A	→	C	N	L	E	C	M	I	R	D
B	→	I	L	D	C	D	J	E	B	C
C	→	H	B	K	N	P	D	H	F	B
D	→	M	O	A	M	Q	E	L	K	P
E	→	K	M	B	G	O	A	F	L	M
F	→	J	E	C	L	M	O	N	E	L
G	→	N	H	N	O	E	P	R	O	H
H	→	R	K	R	Q	N	G	B	P	I
I	→	G	P	J	D	F	R	G	C	K
J	→	P	Q	G	A	L	K	A	M	O
K	→	B	I	Q	P	H	Q	C	D	E
L	→	O	D	M	I	B	C	D	H	G
M	→	L	J	H	K	I	L	K	J	Q
N	→	D	A	F	J	G	F	P	G	A
O	→	A	G	E	H	R	I	J	I	J
P	→	E	F	I	R	J	N	M	Q	N
Q	→	F	R	O	B	A	H	O	A	F
R	→	Q	C	P	F	K	B	Q	N	R

*: Question follows previous

A. Represent 10010111_2 in hexadecimal.
[*Represente* 10010111_2 *em hexadecimal.*]

[1]: 97 [2]: A6 [3]: 83
[4]: 223 [5]: 4B [6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Answer	Version	1	2	3	4	5	6	7	8	9
[1]	→	[5]	[1]	[4]	[3]	[2]	[3]	[2]	[4]	[2]
[2]	→	[4]	[5]	[3]	[4]	[1]	[4]	[4]	[2]	[3]
[3]	→	[3]	[3]	[2]	[2]	[4]	[2]	[5]	[3]	[4]
[4]	→	[2]	[4]	[5]	[1]	[3]	[5]	[3]	[5]	[1]
[5]	→	[1]	[2]	[1]	[5]	[5]	[1]	[1]	[1]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

B. Represent 253_8 in base 10.
[*Represente* 253_8 *na base 10.*]

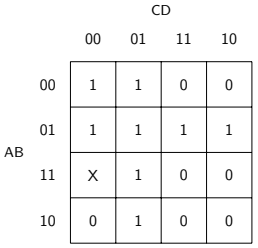
[1]: 171 [2]: 152 [3]: 201
[4]: 339 [5]: 352 [6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Answer	Version	1	2	3	4	5	6	7	8	9
[1]	→	[5]	[2]	[3]	[2]	[4]	[5]	[2]	[4]	[1]
[2]	→	[4]	[1]	[1]	[3]	[2]	[2]	[4]	[2]	[3]
[3]	→	[2]	[4]	[4]	[1]	[1]	[3]	[5]	[1]	[2]
[4]	→	[1]	[3]	[5]	[4]	[3]	[1]	[1]	[5]	[4]
[5]	→	[3]	[5]	[2]	[5]	[5]	[4]	[3]	[3]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

C. Which of the following expressions corresponds to the minimal function (defined as a product-of-sums) represented in the Karnaugh-map?
[*Qual das seguintes expressões corresponde à função mínima (definida como um produto de somas) representada no mapa de Karnaugh?*]



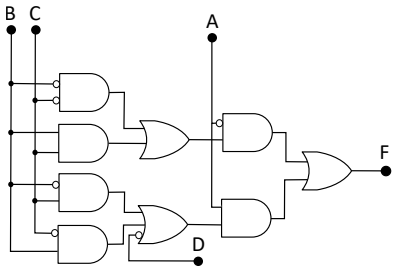
[1]: $(A+\overline{B})(\overline{B}+D)(\overline{B}+\overline{A})$
[2]: $(\overline{A}+C)(\overline{B}+\overline{D})(C+\overline{A})$
[3]: $(B+\overline{C})(\overline{B}+D)(C+\overline{D})$
[4]: $(\overline{B}+D)(A+\overline{C})(\overline{B}+\overline{D})$
[5]: $(B+\overline{C})(\overline{A}+\overline{C})(\overline{A}+D)$
[6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [5]

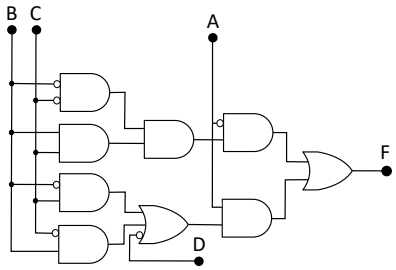
Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[4]	[4]	[4]	[5]	[3]	[3]	[1]	[5]	[4]
[2]	→	[3]	[5]	[3]	[1]	[2]	[5]	[2]	[1]	[2]
[3]	→	[5]	[2]	[5]	[3]	[1]	[1]	[4]	[3]	[5]
[4]	→	[2]	[3]	[1]	[2]	[5]	[4]	[5]	[4]	[3]
[5]	→	[1]	[1]	[2]	[4]	[4]	[2]	[3]	[2]	[1]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

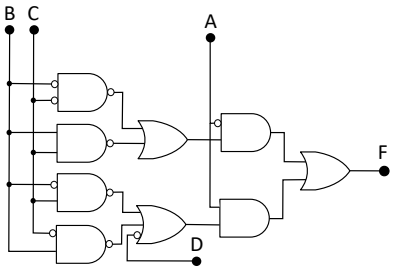
D. Which of the following circuits implements the expression $A \oplus B \oplus \overline{C} + \overline{D}A$?
[*Qual dos seguintes circuitos implementa a expressão* $A \oplus B \oplus \overline{C} + \overline{D}A$*?*]



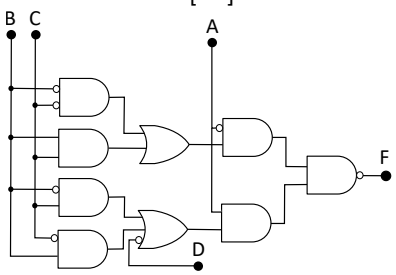
[1]



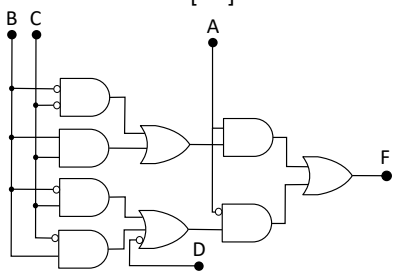
[2]



[3]



[4]



[5]

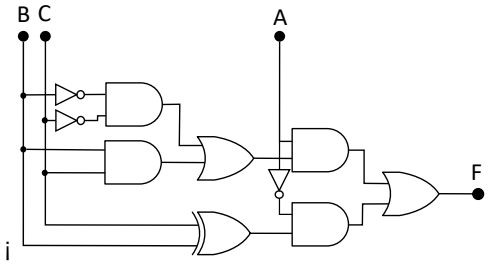
None of the other options
[*Nenhuma das outras opções*]
[6]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[1]	[5]	[1]	[1]	[5]	[3]	[1]	[2]	[3]
[2]	→	[4]	[2]	[3]	[2]	[1]	[5]	[3]	[1]	[4]
[3]	→	[5]	[4]	[5]	[5]	[2]	[4]	[2]	[5]	[2]
[4]	→	[2]	[3]	[2]	[3]	[3]	[2]	[5]	[4]	[1]
[5]	→	[3]	[1]	[4]	[4]	[4]	[1]	[4]	[3]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

E. What is the worst case for the propagation time of the following circuit?
[*Qual é o pior caso para o tempo de propagação do seguinte circuito?*]



Gate	tp [ns]
NOT	4
AND	8
OR	7
XOR	11

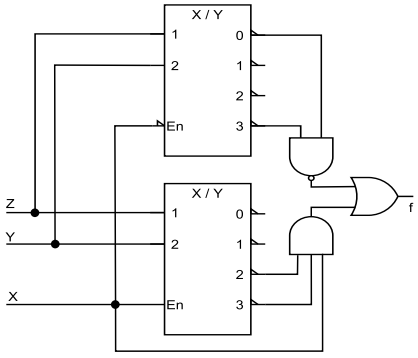
[1]: 34 [2]: 26 [3]: 38
[4]: 30 [5]: 50 [6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[3]	[3]	[5]	[4]	[3]	[1]	[2]	[4]	[2]
[2]	→	[2]	[5]	[4]	[1]	[4]	[2]	[4]	[3]	[3]
[3]	→	[5]	[4]	[2]	[3]	[2]	[5]	[5]	[2]	[4]
[4]	→	[4]	[2]	[3]	[2]	[1]	[4]	[3]	[1]	[5]
[5]	→	[1]	[1]	[1]	[5]	[5]	[3]	[1]	[5]	[1]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

F. Select the option corresponding to the output $f(X,Y,Z)$ of the circuit shown below, when the inputs (X,Y,Z) have the values $(0,0,1)$,$(0,1,1)$, and $(1,1,0)$.
[*Indique qual das opções corresponde à saída* $f(X,Y,Z)$ *do circuito apresentado em baixo, quando as entradas* (X,Y,Z) *tomam os valores* $(0,0,1)$,$(0,1,1)$, *e* $(1,1,0)$.]



[1]: $\{f(0,0,1)\ ;\ f(0,1,1)\ ;\ f(1,1,0)\} = \{0\ ;\ 0\ ;\ 1\}$
[2]: $\{f(0,0,1)\ ;\ f(0,1,1)\ ;\ f(1,1,0)\} = \{0\ ;\ 1\ ;\ 1\}$
[3]: $\{f(0,0,1)\ ;\ f(0,1,1)\ ;\ f(1,1,0)\} = \{1\ ;\ 0\ ;\ 0\}$
[4]: $\{f(0,0,1)\ ;\ f(0,1,1)\ ;\ f(1,1,0)\} = \{1\ ;\ 0\ ;\ 1\}$
[5]: $\{f(0,0,1)\ ;\ f(0,1,1)\ ;\ f(1,1,0)\} = \{0\ ;\ 1\ ;\ 0\}$
[6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [5]

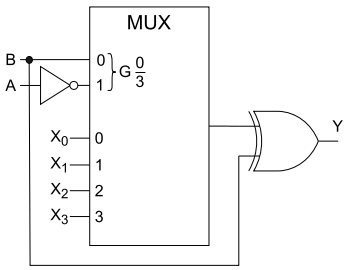
Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[4]	[5]	[2]	[2]	[3]	[4]	[4]	[2]	[5]
[2]	→	[5]	[4]	[4]	[1]	[1]	[2]	[2]	[3]	[1]
[3]	→	[3]	[3]	[1]	[3]	[5]	[3]	[1]	[5]	[3]
[4]	→	[2]	[1]	[3]	[4]	[4]	[5]	[5]	[4]	[2]
[5]	→	[1]	[2]	[5]	[5]	[2]	[1]	[3]	[1]	[4]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

G. Consider the following circuit and truth table. Select the multiplexer inputs $\{X_3; X_2; X_1; X_0\}$ that result in the given truth table.
[*Considere o seguinte circuito e tabela de verdade. Selecione as entradas do multiplexer* $\{X_3; X_2; X_1; X_0\}$ *que resultam na tabela apresentada.*]

[1]: $\{X_3; X_2; X_1; X_0\} = \{1; C; C; 1\}$
[2]: $\{X_3; X_2; X_1; X_0\} = \{\overline{C}; 0; C; C\}$
[3]: $\{X_3; X_2; X_1; X_0\} = \{C; \overline{C}; 1; C\}$
[4]: $\{X_3; X_2; X_1; X_0\} = \{\overline{C}; 1; \overline{C}; C\}$
[5]: $\{X_3; X_2; X_1; X_0\} = \{\overline{C}; C; \overline{C}; 1\}$
[6]: None of the other options
[*Nenhuma das outras opções*]

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



Correct answers: [1]
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1] →	[4]	[5]	[1]	[3]	[1]	[4]	[2]	[3]	[4]
[2] →	[1]	[2]	[3]	[1]	[4]	[3]	[5]	[1]	[3]
[3] →	[2]	[3]	[5]	[5]	[5]	[1]	[1]	[2]	[5]
[4] →	[3]	[1]	[2]	[2]	[2]	[5]	[3]	[5]	[2]
[5] →	[5]	[4]	[4]	[4]	[3]	[2]	[4]	[4]	[1]
[6] →	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

H. What is the 8-bit two's complement representation of -99?
[*Qual é a representação em complemento para dois com 8-bits de* -99*?*]

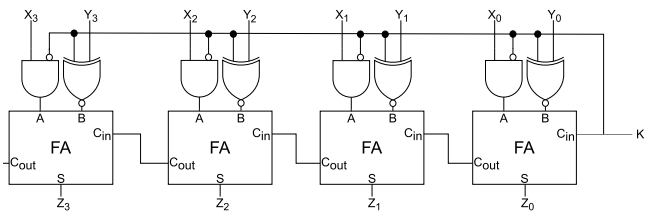
[1]: 10011101 [2]: 10011100 [3]: 11000110
[4]: 00110101 [5]: 10110011 [6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [1]
Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1] →	[5]	[1]	[3]	[5]	[5]	[3]	[3]	[5]	[1]
[2] →	[1]	[5]	[4]	[2]	[4]	[1]	[2]	[1]	[4]
[3] →	[2]	[2]	[2]	[1]	[2]	[5]	[5]	[2]	[2]
[4] →	[3]	[4]	[1]	[3]	[3]	[2]	[4]	[4]	[5]
[5] →	[4]	[3]	[5]	[4]	[1]	[4]	[1]	[3]	[3]
[6] →	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

I. Which function is implemented by the following circuit? Consider that X and Y are 4-bit signed numbers (two's complement).
[*Qual é a função desempenhada pelo seguinte circuito? Assuma que X e Y são números com sinal com 4-bits (em complemento para dois).*]

[1]: K=0: Z=X-Y-1 ; K=1: Z=Y+1
[2]: K=0: Z=X+Y ; K=1: Z=Y-1
[3]: K=0: Z=X-1 ; K=1: Z=X+Y
[4]: K=0: Z=X+1 ; K=1: Z=X-Y
[5]: K=0: Z=X+2 ; K=1: Z=Y-2
[6]: None of the other options
[*Nenhuma das outras opções*]

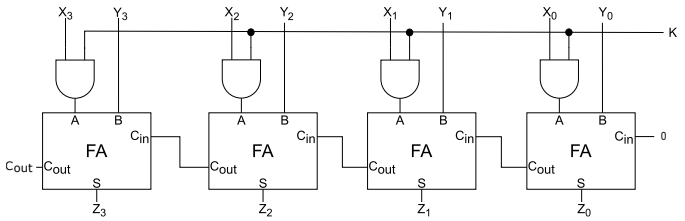


Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1] →	[3]	[5]	[4]	[5]	[1]	[2]	[3]	[5]	[5]
[2] →	[4]	[2]	[1]	[2]	[2]	[4]	[1]	[1]	[3]
[3] →	[1]	[1]	[3]	[1]	[3]	[3]	[5]	[2]	[2]
[4] →	[2]	[4]	[2]	[3]	[4]	[1]	[2]	[4]	[4]
[5] →	[5]	[3]	[5]	[4]	[5]	[5]	[4]	[3]	[1]
[6] →	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

J. What is the worst case for the propagation time of the following circuit?
[*Qual é o pior caso para o tempo de propagação do seguinte circuito?*]



Gate	tp [ns]
AND	7

FA propagation times (ns)

	S	cout
A/B	20	24
cin	14	10

[1]: 75
[2]: 43
[3]: 81
[4]: 65
[5]: 90
[6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [4]

Answer permutations: (All answers permuted, except last answer)

Version	1	2	3	4	5	6	7	8	9
Answer									
[1] →	[2]	[4]	[3]	[3]	[2]	[2]	[4]	[2]	[4]
[2] →	[3]	[2]	[2]	[5]	[1]	[4]	[5]	[1]	[1]
[3] →	[4]	[3]	[5]	[2]	[5]	[1]	[1]	[4]	[5]
[4] →	[1]	[1]	[4]	[4]	[3]	[3]	[2]	[5]	[2]
[5] →	[5]	[5]	[1]	[1]	[4]	[5]	[3]	[3]	[3]
[6] →	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

K. Consider the following state transition table (one-hot encoding) with two inputs $Init$ and X, two outputs $Y1$ and $Y0$, where each state $S_i (i = 0, ..., 3)$ is implemented with D flip-flops, with input D_i (next state) and output Q_i (current state). Select, only for the state S_3, the correct option for D_3 as a function of $Init$ and X and the current states Q_i.
[*Considere a seguinte tabela de transição de estados (codificação one-hot) com duas entradas $Init$ e X, duas saídas $Y1$ e $Y0$, em que cada estado $S_i (i = 0, ..., 3)$ é implementad0 com flip-flops do tipo D, com entradas D_i (próximo estado) e saídas Q_i (estado actual). Indique, para o estado S_3, a expressão de D_3 como função de $Init$ e X e os estados actuais Q_i.*]

Q3(n)	Q2(n)	Q1(n)	Q0(n)	Init	X	Q3(n+1)	Q2(n+1)	Q1(n+1)	Q0(n+1)	Y1	Y0
0	0	0	1	0	0	1	0	0	0	0	1
0	0	0	1	0	1	0	1	0	0	1	1
0	0	1	0	0	0	1	0	0	0	0	0
0	0	1	0	0	1	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	1	0	0	1
1	0	0	0	0	0	1	0	0	0	1	1
1	0	0	0	0	1	0	1	0	0	0	0
-	-	-	-	1	-	0	1	0	0	0	0

[1]: $D_3 = \overline{Init} \cdot \overline{X} \cdot (Q_0 + Q1 + Q3)$

[2]: $D_3 = \overline{Init} \cdot (\overline{X} \cdot Q_0 + \overline{X} \cdot Q2 + X \cdot Q3)$

[3]: $D_3 = X \cdot Q_0 + \overline{X} \cdot Q2 \cdot Y_1 + X \cdot Q3 \cdot Y_0$

[4]: $D_3 = Init + X \cdot Q_0 + \overline{X} \cdot Q1 + X \cdot Q2$

[5]: $D_3 = X \cdot Q_1 + \overline{X} \cdot Q2 \cdot Y_0 + X \cdot Q3$

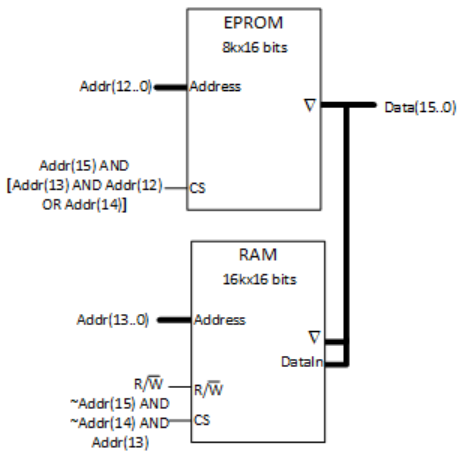
[6]: None of the other options
[*Nenhuma das outras opções*]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[4]	[5]	[1]	[4]	[2]	[3]	[1]	[1]	[5]
[2]	→	[5]	[4]	[4]	[5]	[1]	[4]	[5]	[5]	[1]
[3]	→	[3]	[3]	[5]	[2]	[5]	[2]	[2]	[3]	[3]
[4]	→	[2]	[2]	[2]	[3]	[4]	[1]	[3]	[2]	[2]
[5]	→	[1]	[1]	[3]	[1]	[3]	[5]	[4]	[4]	[4]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

L. Consider the following memory system. Indicate the range of addresses that correspond to RAM and EPROM.
[*Considere o seguinte sistema de memória. Indique os intervalos de endereços que correspondem a RAM e EPROM.*]



[1]: EPROM:8000h..BFFFh; RAM:1000h..2FFFh

[2]: EPROM:B000h..FFFFh; RAM:2000h..3FFFh

[3]: EPROM:8000h..BFFFh; RAM:2000h..3FFFh

[4]: EPROM:B000h..EFFFh; RAM:1000h..2FFFh

[5]: EPROM:C000h..FFFFh; RAM:1000h..2FFFh

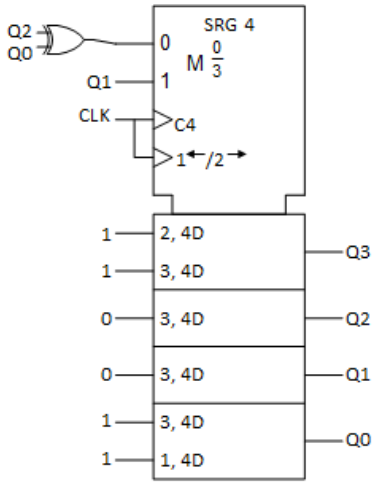
[6]: None of the other options
[*Nenhuma das outras opções*]

Correct answers: [2]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[4]	[5]	[3]	[2]	[4]	[3]	[4]	[3]	[3]
[2]	→	[2]	[2]	[2]	[3]	[1]	[5]	[1]	[2]	[2]
[3]	→	[3]	[3]	[1]	[1]	[2]	[1]	[2]	[5]	[1]
[4]	→	[1]	[4]	[5]	[4]	[5]	[4]	[3]	[4]	[5]
[5]	→	[5]	[1]	[4]	[5]	[3]	[2]	[5]	[1]	[4]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

M. Consider the following circuit with a 4-bit shift register, as depicted in the figure. The current state is Q3 Q2 Q1 Q0 = 1011. What are the next two states of the circuit?
[*Considere o seguinte circuito com um registo de deslocamento de 4-bits representado na figura. O estado actual é Q3 Q2 Q1 Q0 = 1011. Quais serão os próximos dois estados?*]



[1]: 1001, 0011

[2]: 0011, 1111

[3]: 1011, 0110

[4]: 1010, 0110

[5]: 1001, 1001

[6]: None of the other options
[*Nenhuma das outras opções*]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[4]	[1]	[1]	[1]	[5]	[3]	[4]	[1]	[1]
[2]	→	[5]	[2]	[3]	[3]	[4]	[4]	[3]	[5]	[3]
[3]	→	[2]	[3]	[2]	[5]	[3]	[2]	[1]	[2]	[2]
[4]	→	[1]	[4]	[4]	[2]	[1]	[1]	[2]	[3]	[4]
[5]	→	[3]	[5]	[5]	[4]	[2]	[5]	[5]	[4]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

N. Consider the following circuit with an adder, a register (4 FF's) and a combinational logic circuit. Assuming that the current state is Q(3:0) = 1010, what are the next two states of the circuit?
[*Considere o seguinte circuito com um somador, um registo (4 FF's) e lógica combinatória. Assumindo que o estado actual é Q(3:0) = 1010, quais serão os próximos dois estados do circuito?*]

[1]: 1001, 0111

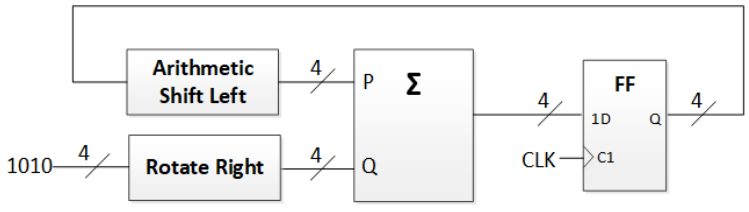
[2]: 1100, 1000

[3]: 0011, 1110

[4]: 1110, 1011

[5]: 0101, 0111

[6]: None of the other options
[*Nenhuma das outras opções*]

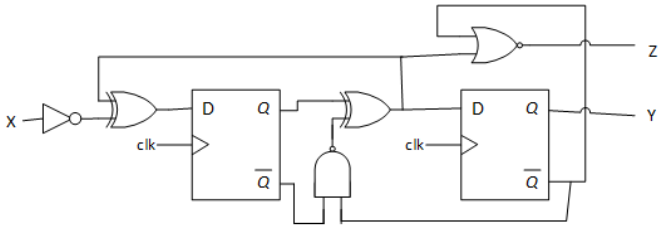


Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[5]	[4]	[3]	[2]	[2]	[5]	[3]	[2]	[3]
[2]	→	[2]	[3]	[5]	[4]	[4]	[3]	[2]	[4]	[4]
[3]	→	[1]	[5]	[2]	[1]	[5]	[4]	[5]	[1]	[2]
[4]	→	[4]	[2]	[4]	[3]	[1]	[1]	[4]	[5]	[1]
[5]	→	[3]	[1]	[1]	[5]	[3]	[2]	[1]	[3]	[5]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

O. What is the minimum clock period of the following circuit, given the table values (in ns)?
[*Qual é o período de relógio mínimo do seguinte circuito, assumindo os valores da tabela (em ns)?*] *



	tp [ns]	tsu [ns]	th [ns]
FF D	14	7	5
NAND	9		
NOR	8		
XOR	12		
NOT	5		

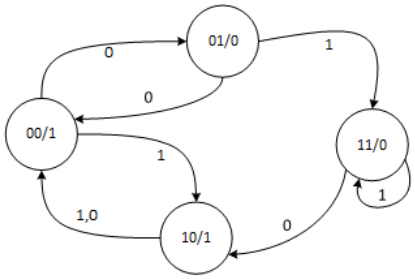
[1]: 54 [2]: 49 [3]: 41
[4]: 59 [5]: 51 [6]: None of the other options [*Nenhuma das outras opções*]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[4]	[4]	[3]	[4]	[3]	[3]	[5]	[3]	[4]
[2]	→	[5]	[1]	[2]	[3]	[1]	[5]	[2]	[1]	[2]
[3]	→	[1]	[2]	[5]	[5]	[5]	[1]	[1]	[2]	[5]
[4]	→	[3]	[3]	[4]	[2]	[2]	[4]	[3]	[4]	[1]
[5]	→	[2]	[5]	[1]	[1]	[4]	[2]	[4]	[5]	[3]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

P. Consider the following state diagram. Select the output value for each state and the value of the next state for each state and input.
[*Considere o seguinte diagrama de estados. Indique o valor da saída do circuito para cada estado e o valor do próximo estado para cada valor do estado e entrada.*]



		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	01	10
01	0	00	11
10	1	00	00
11	0	10	11

[1]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	10	10
01	1	00	11
10	1	01	01
11	0	01	11

[2]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	0	10	00
01	1	10	11
10	0	10	01
11	1	11	01

[3]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	10	01
01	0	11	10
10	0	00	00
11	1	01	01

[4]

		Q(n+1)	Q(n+1)
Q(n)	Y(n)	x=0	x=1
00	1	10	01
01	0	11	10
10	1	00	00
11	1	01	01

[5]

None of the other options
[*Nenhuma das outras opções*]

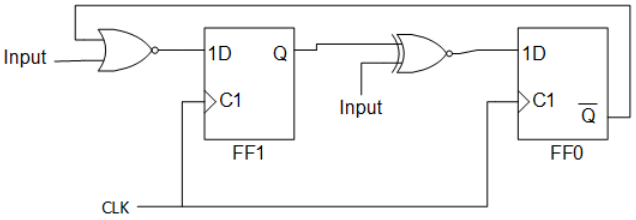
[6]

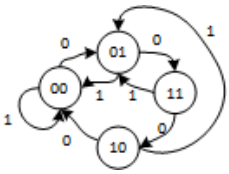
Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

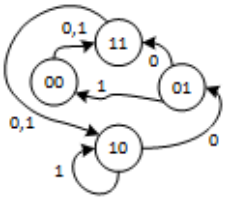
Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[2]	[1]	[5]	[2]	[5]	[2]	[3]	[2]	[4]
[2]	→	[1]	[3]	[3]	[3]	[2]	[1]	[2]	[4]	[1]
[3]	→	[4]	[5]	[1]	[1]	[1]	[4]	[1]	[1]	[5]
[4]	→	[5]	[4]	[2]	[4]	[4]	[5]	[4]	[5]	[2]
[5]	→	[3]	[2]	[4]	[5]	[3]	[3]	[5]	[3]	[3]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

Q. Consider the following circuit. Which state diagram corresponds to the circuit?
[*Considere o seguinte circuito. Qual dos diagramas de estado corresponde ao funcionamento do circuito?*]

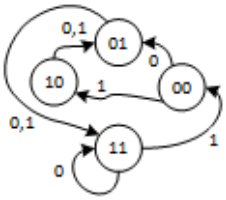




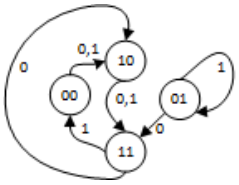
[1]



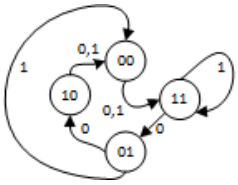
[2]



[3]



[4]



[5]

None of the other options
[*Nenhuma das outras opções*]

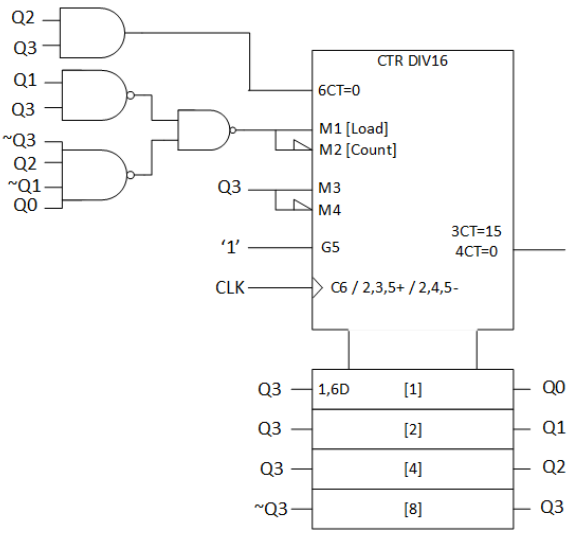
[6]

Correct answers: [1]

Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[3]	[2]	[1]	[3]	[1]	[3]	[1]	[4]	[4]
[2]	→	[5]	[5]	[3]	[2]	[2]	[5]	[5]	[2]	[1]
[3]	→	[1]	[1]	[2]	[5]	[3]	[4]	[3]	[1]	[5]
[4]	→	[4]	[4]	[5]	[4]	[4]	[1]	[4]	[5]	[2]
[5]	→	[2]	[3]	[4]	[1]	[5]	[2]	[2]	[3]	[3]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

R. Which of the following options corresponds to the sequence, in stationary mode, in decimal format at the output of the circuit in the figure below? (suggestion: start by analyzing a "load" situation.)
[*Qual das seguintes opções corresponde à sequência de saída do seguinte circuito, em regime estacionário e em formato decimal? (sugestão: começe por analisar a situação de carregamento ("load") de dados.)*]



[1]: ... 10 - 7 - 6 - 5 - 8 - 9 - 10 ...

[2]: ... 12 - 1 - 2 - 3 - 14 - 13 - 12 ...

[3]: ... 14 - 3 - 2 - 1 - 12 - 13 - 14 ...

[4]: ... 11 - 3 - 4 - 5 - 13 - 12 - 11 ...

[5]: ... 13 - 5 - 4 - 3 - 11 - 12 - 13 ...

[6]: None of the other options
[*Nenhuma das outras opções*]

Correct answers: [1]

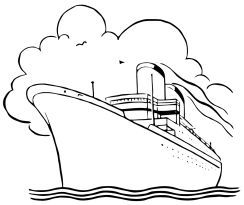
Answer permutations: (All answers permuted, except last answer)

Version		1	2	3	4	5	6	7	8	9
Answer										
[1]	→	[1]	[3]	[5]	[1]	[5]	[2]	[5]	[3]	[5]
[2]	→	[4]	[5]	[2]	[2]	[1]	[3]	[2]	[4]	[4]
[3]	→	[5]	[4]	[1]	[5]	[4]	[1]	[4]	[5]	[2]
[4]	→	[3]	[1]	[4]	[3]	[2]	[4]	[1]	[1]	[1]
[5]	→	[2]	[2]	[3]	[4]	[3]	[5]	[3]	[2]	[3]
[6]	→	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]	[6]

(This space was intentionally left blank for you auxiliary calculations.)

Volume 1 - Part II

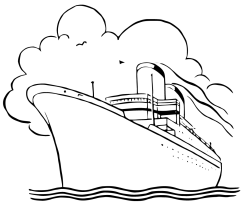
NOTE: Portuguese version in the following [Question score partitioning: 33% + 34% + 33%]



A ship has two cargo holds that allow it to carry 10 tons of grain each. Two sensors provide the weight in each of the holds in tons. Using the discrete logic you find necessary and the indicated components, answer the following questions.

1. Knowing that each of the sensors has a 6-bit signal output (signals P_a and P_b), draw the circuit that calculates the total weight of the cereals transported by the ship in tons (8-bit P_t) using 4-bit adders.
2. Knowing that one of the cargo holds (P_a) takes wheat that occupies 0.5 m^3 per ton and the other takes rye (P_b) that occupies 1.25 m^3 per ton, draw the circuit that determines the total volume (V of 8 bits) occupied by the cereals in m^3. Use 8-bit adders and round the result to the largest integer less than or equal to the actual value (that is, round down).
3. Draw the circuit that allows you to determine if, in some of the holds (one or the other), the weight is greater than the 10 tons allowed in each. Use 8-bit adders, and do not use comparators.

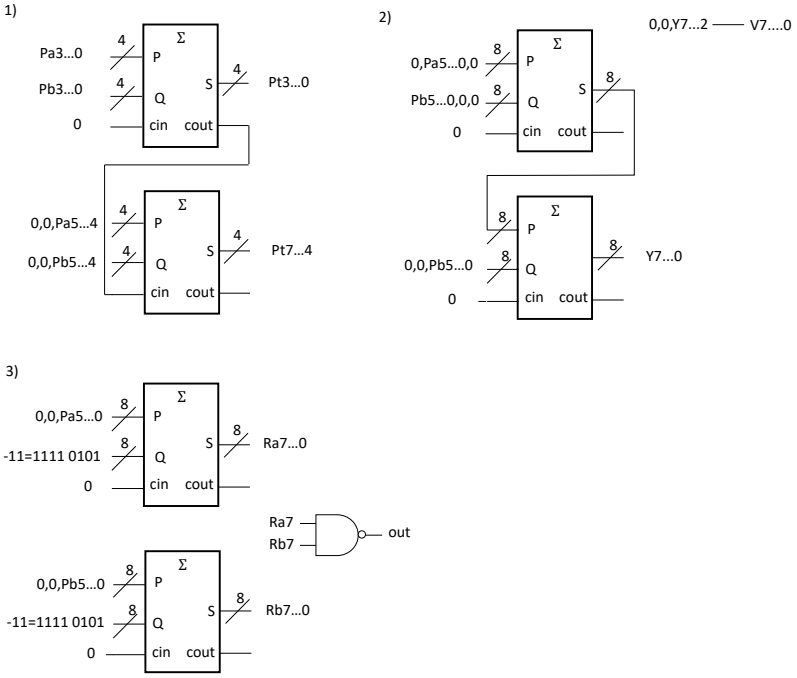
Portuguese version:



Um navio tem dois porões que permitem carregar 10 toneladas de cereais cada um, e dois sensores que fornecem o peso em cada um dos porões em toneladas. Utilizando a lógica discreta que achar necessária e os componentes indicados responda às seguintes perguntas.

1. Sabendo que cada um dos sensores tem como saída um sinal de 6 bits com sinal (sinais P_a e P_b), desenhe o circuito que calcula o peso total de cerais transportado pelo navio em toneladas, (P_t de 8 bits) usando somadores de 4 bits.
2. Sabendo que um dos porões leva trigo que ocupa 0.5 m^3 por tonelada e o outro leva centeio que ocupa 1,25 m^3 por tonelada, desenhe o circuito que determina o volume total (V de 8 bits) ocupado pelos cereais em m^3. Utilize somadores de 8 bits e arredonde o resultado para o maior inteiro menor ou igual que o valor real (ou seja, arredonde para baixo).
3. Desenhe o circuito que permite determinar se, em alguns dos porões (num ou no outro), o peso é maior do que as 10 toneladas permitidas em cada. Utilize somadores de 8 bits e não use comparadores.

Solução Proposta:



Volume 1 - Part III

NOTE: Portuguese version in the following page [Question score partitioning: 50% + 50%]

Design a circuit that controls access to a room that is adjacent to a chemical reactor. In case of a toxic gas leak is detected, an automated safety door isolates the room to prevent spread of contamination to other parts of the building. The control mechanism to be developed works as follows:

- All the signals are Active High.
- Input signal B comes from a button-switch used to manually activate the safety mechanism. Input signal SC is activated when the chemical sensor detects toxic gases. Input signal SD is activated when the door is completely closed. Input signal T is activated when one of the system timers expires (see below).
- There are two timers, Timer 1 with length T1, and Timer 2 with length T2. Output signal AT1 activates Timer 1. Output signal AT2 activates Timer 2. Each of the timers is activated when the respective activation signal (AT1 or AT2) makes a transition from '0' to '1'. The timer is deactivated in case the respective activation signal returns to value '0'. Only one of the timers may be active at each time, since signal T is common to both. In case of simultaneous activation of AT1 and AT2, signal T will not be activated.
- Output signal AS activates an alarm sound. Output signal RL activates a red light. Output signal DC opens the door when active, closing it otherwise.
- The control mechanism starts in a disabled state, where the door stays open. The activation of button B enables the safety system. From here, while toxic gases are not detected, the door remains open and the red light switched off.
- Upon detection of toxic gases, the red light is be permanently on, and the door closing mechanism will be permanently activated. While the door is being closed, the alarm will sound intermittently, with equal intervals of sound and silence of length T1.
- Once the door is completely closed, the alarm sound will stop and the red light will be on for at least T2. After this time interval, the red light will be switched off once the gases cease to be detected. However, the door will remain closed. In this state, in case the toxic gases are detected again, the red light will be again switched on.
- The system can return to the initial state by deactivating B, but only in states where the red light switched is off.

Consider the incomplete state diagram of the Moore machine of the circuit (see Volume 2, Part III).

Complete the diagram, defining the values of the input signals associated with all state transitions, as well as the values of the output signals associated with each state. "Don't cares" must be used for the inputs whose value does not matter for given a state transition. In the diagram, indicate the inputs/outputs according to the following order:

- Order of the inputs: B, SC, SD, T.
- Order of the outputs: AT1, AT2, AS, RL, DC.

Question B:

The state transition table on the right describes the behavior of a machine with 4 states, one input E and one output Y. A circuit that implements it using two flip-flops of type D (FF0 and FF1), as well as AND, OR and NOT gates, is to be projected. Obtain the logical expressions (in minimal disjunctive form) for the flip-flop input signals, as well as the output of the circuit.

Q1(n)	Q0(n)	E	Q1(n+1)	Q0(n+1)	Y
0	0	0	0	1	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	1	1	0

D0 = ... D1 = ... Y = ...

Pergunta A:

Projete um circuito que controla o acesso a uma sala adjacente a um reator químico. Em caso de fuga de gases tóxicos, uma porta de segurança automática isola a sala para prevenir contaminação de outras partes do edifício. O mecanismo de controlo a projetar funciona da forma seguinte:

- Todos os sinais são Ativos a High.
- O sinal de entrada B está associado a um interruptor de botão utilizado para ativar manualmente o mecanismo de segurança. O sinal de entrada SC é ativado quando o sensor químico deteta gases tóxicos. O sinal de entrada SD é ativado quando a porta está completamente fechada. O sinal de entrada T é ativado quando um dos temporizadores do sistema expira (ver abaixo).
- Existem dois temporizadores, Timer 1 com duração T1, e Timer 2 com duração T2. O sinal de saída AT1 ativa Timer 1. O sinal de saída AT2 ativa Timer 2. Cada um dos temporizadores é ativado quando o respetivo sinal de ativação (AT1 ou AT2) transita de '0' para '1'. O temporizador é desativado caso o respetivo sinal de ativação regresse ao valor '0'. Apenas um dos temporizadores pode estar ativo de cada vez, pois o sinal T é comum a ambos. Caso os sinais AT1 e AT2 sejam ativados simultaneamente, o sinal T não será ativado.
- O sinal de saída AS ativa um alarme sonoro. O sinal de saída RL ativa uma luz vermelha. O sinal de saída DC abre a porta quando está ativo, fechando-a no caso contrário.
- O sistema de controlo começa no estado inativo, em que a porta permanece aberta. A ativação do botão B ativa o sistema de segurança. A partir daqui, enquanto não forem detetatos gases tóxicos, a porta permanece aberta e a luz vermelha apagada.
- Uma vez detetados gases tóxicos, a luz vermelha fica permanentemente ligada, e o sistema de fecho da porta fica permanentemente ativado. Enquanto a porta está a fechar, o alarme vai soar intermitentemente, com intervalos iguais de som e silêncio de duração T1.
- Uma vez que a porta esteja completamente fechada, o alarme sonoro para, e a luz vermelha ficará acesa durante, pelo menos, T2. Depois deste intervalo, a luz vermelha será desligada quando já não forem detetados gases. No entanto, a porta permanecerá fechada. Neste estado, caso voltem a ser detetados gases tóxicos, a luz vermelha voltará a acender.
- O sistema pode voltar ao estado inicial desativando B, mas apenas em estados em que a luz vermelha esteja apagada.

Considere o diagrama de estados incompleto da máquina de Moore do circuito (ver Volume 2, Parte III). Complete o diagrama, definindo os valores dos sinais de entrada que desencadeiam todas as transições de estado, assim como os valores de saída de cada estado. As "indiferenças" têm de ser obrigatoriamente usadas para entradas que não tenham influência numa determinada transição de estado. As entradas/saídas têm de ser indicadas de acordo com a ordem seguinte:

- Ordem das entradas: B, SC, SD, T.
- Ordem das saídas: AT1, AT2, AS, RL, DC.

Pergunta B:

A tabela de transição de estados à direita descreve uma máquina com 4 estados, uma entrada E e uma saída Y. Projecte o circuito que a implementa utilizando dois flip-flops D (FF0 e FF1), assim como portas AND, OR e NOT. Obtenha as expressões algébricas (na forma mínima disjuntiva) para os sinais de entrada dos flip-flops, assim como da saída do circuito.

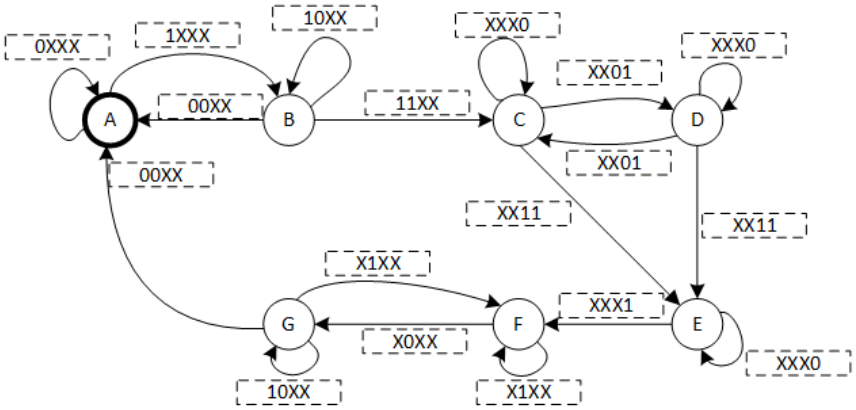
Q1(n)	Q0(n)	E	Q1(n+1)	Q0(n+1)	Y
0	0	0	0	1	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	1	1	0

D0 = ... D1 = ... Y = ...

Solução Proposta:

A: Initial state, disabled [Estado inicial, sistema inativo];
B: Enabled, no gases, door open [Ativo, sem gases, porta aberta];
C: Enabled, gas detected, sounding alarm, closing door [Ativo, gases detetatos, alarme a tocar, a fechar porta];
D: Enabled, gas detected, alarm not sounding, closing door [Ativo, gases detetatos, alarme em silêncio, a fechar porta];
E: Enabled, door closed, Timer2 active [Ativo, porta fechada, Timer2 ativo];
F: Enabled, gas detected, Timer2 expired [Ativo, gases detetatos, Timer2 expirado];
G: Enabled, no gases, waiting disablement or gas detection to restart [Ativo, sem gases, aguarda desativação ou deteção de gases para reiniciar];

- Order of the inputs[Ordem das entradas]: B, SC, SD, T.
- Order of the outputs[Ordem das saídas]: AT1, AT2, AS, RL, DC.



A: 00001
B: 00001
C: 10110
D: 10010
E: 01010
F: 00010
G: 00000

Q1(n)	Q0(n)	E	Q1(n+1)=D1	Q0(n+1)	Y
0	0	0	0	1	0
0	0	1	1	0	1
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	1	1	0

Q1Q0/E	0	1
00	0	1
01	0	1
11	1	1
10	0	0

D1

Q1Q0/E	0	1
00	1	0
01	1	1
11	0	1
10	1	0

D0

Q1Q0/E	0	1
00	0	1
01	1	0
11	1	0
10	0	1

Y

D1 = ~Q1E+Q1Q0

D0 = ~Q0~E+~Q1~E+Q0E

Y = Q0~E+~Q0E

Don't forget to identify this and the following pages!
Only these pages will be considered for your evaluation.

Volume 2 - Part I

For each question of Part I (question A, B, C, ...), fill in the number of the **correct answer** from the supplied multiple-choice list (answer 1, 2, 3, ...):

⋆	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1																			X	X	X	X	X	X	X	X

NOTE: Leave blank (or fill in with 0) all questions that you do not wish to answer.

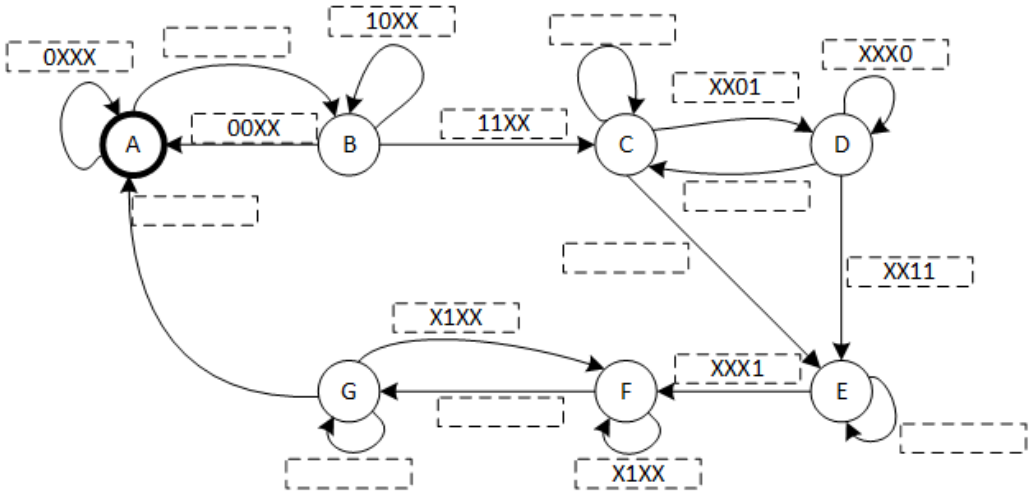
Volume 2 - Part II

Volume 2 - Part II (Cont.)

Volume 2 - Part III

Meaning of the states [*Significado dos estados*]:

- A: Initial state, disabled, door open [*Estado inicial, sistema inactivo*];
- B: Enabled, no gases, door open [*Ativo, sem gases, porta aberta*];
- C: Enabled, gas detected, sounding alarm, closing door [*Ativo, gases detetatos, alarme a tocar, a fechar porta*];
- D: Enabled, gas detected, alarm not sounding, closing door [*Ativo, gases detetatos, alarme em silêncio, a fechar porta*];
- E: Enabled, door closed, Timer2 active [*Ativo, porta fechada, Timer2 ativo*];
- F: Enabled, gas detected, Timer2 expired [*Ativo, gases detetatos, Timer2 expirado*];
- G: Enabled, no gases, waiting disablement or detection to restart [*Ativo, sem gases, aguarda desativação ou deteção de gases para reiniciar*];



For each state, define the values of the inputs (in the diagram) and of the outputs (below) according to the following order: [*Para cada estado, indique os valores das entradas (no diagrama) e das saídas (em baixo) de acordo com a seguinte ordem*]:

- Order of the inputs[*Ordem das entradas*]: B, SC, SD, T.
- Order of the outputs[*Ordem das saídas*]: AT1, AT2, AS, RL, DC.

- A: _____
- B: _____
- C: _____
- D: _____
- E: _____
- F: _____
- G: _____

Volume 2 - Part III (Cont.)